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APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. 09/031,326 02/26/98 KARNIEWICZ J 303.376051

-021186 LM01/1110 SCHWEGMAN LUNDBERG WOESSNER & KLUTH P O BOX 2938 MINNEAPOLIS MN 55402 FHAN, I

ART UNIT PAPER NUMBER 2763

DATE MAILED:

11/10/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No. 09/031,326

Applicant(s,

Joseph J. Karnlewicz

Examiner

Thai Phan

Group Art Unit 2763



Responsive to communication(s) filed on	·
☐ This action is FINAL.	
☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quay#835 C.D. 11; 453 O.G. 213.	
A shortened statutory period for response to this action is set to explonger, from the mailing date of this communication. Failure to respapplication to become abandoned. (35 U.S.C. § 133). Extensions 37 CFR 1.136(a).	oond within the period for response will cause the
Disposition of Claim	
	is/are pending in the applicat
Of the above, claim(s)	is/are withdrawn from consideration
☐ Claim(s)	is/are allowed.
X Claim(s) <u>1-25</u>	
Claim(s)	
	are subject to restriction or election requirement.
Application Papers See the attached Notice of Draftsperson's Patent Drawing Remainders on the control of the description of the control of t	
☐ The drawing(s) filed on is/are object	
☐ The proposed drawing correction, filed on is ☐ approved ☐ disapproved.	
☐ The specification is objected to by the Examiner.	
☐ The oath or declaration is objected to by the Examiner.	
Priority under 35 U.S.C. § 119 Acknowledgement is made of a claim for foreign priority und All Some* None of the CERTIFIED copies of the	
received.	
 ☐ received in Application No. (Series Code/Serial Number) ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)). 	
Attachment(s)	
Notice of References Cited, PTO-892	•
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)
☐ Interview Summary, PTO-413	
☐ Notice of Draftsperson's Patent Drawing Review, PTO-948	
☐ Notice of Informal Patent Application, PTO-152	
SEE OFFICE ACTION ON THE FOLLOWING PAGES	

Art Unit: 2763

DETAILED ACTION

This official action is in response to patent application S/N: 09/031,326. Claims 1-25 are pending in this official action.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show labels of functional blocks as described in the specification such as in Figs. 1, 3, 4. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

Claim Rejections - 35 USC § 102

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ahmed, Sultan, patent number 5,455,938.

As per claim 1, Ahmed disclosed method and system for generating test instructions for testing integrated circuit using a database structure for storing and accessing data (Abstract, Fig. 1) identical to the claimed invention. According to Ahmed, the system includes a global file of global variables (col. 5, line 50 to col. 6, line 35), a plurality of local files relating to local variables to the global variables (col. 7, line 55 to col. 8, line 64, col. 9, lines 44-53, for instance), and local files in the templates containing a plurality of cells as inherently known in the art.

As per claims 2, 3, 10, and 11 diagnostic files of global files or local files contain inherit files and instance files (col. 8, lines 55-64) to fill in or change parameters in each file.

Art Unit: 2763

As per claim 4, Ahmed discloses files such as diagnostic files, netlist files, state files, etc. as in blocks 82, 86, 56, 58, 60 would also include master file to keep design parameters in these files as known for those skilled in the art.

As per claim 5, Ahmed discloses various templates or platforms being used for the design verification. This would also clean sheet files as known for those skilled in the art to generate a new design file, including global variables, design parameters, for example.

As per claims 6, 8, 9 and 12, Ahmed discloses file update or modifying design file for circuit design verification (col. 7, lines 35-55, col. 9, lines 45-53, col. 11, lines 8-25, cols. 12, 13, for instance) which has been well-known for those skilled in the art. The update process is carried out in local files, fields, global files, design rule files as necessarily required by the verification process (col. 12, 13, line 11 to col. 15, line 4).

As per claims 7 and 13, Ahmed discloses change of parameter values. This would require means for entering new values for parameters, variables, etc., and means for displaying of parameter value change (Fig. 1).

As per claim 14, Ahmed discloses computerized system for implementing design verification. Ahmed requires the process verification is implemented in a computer programming language, but Ahmed does not expressly disclose the specific computer programming language SKILL as claimed. SKILL programming language in conjunction with Design Framework II as claimed is known in the art as especially used by applicants. It would be obvious for practitioner in the art to use such available tool to implement the design verification process as taught by Ahmed to provide an efficient method to implement the verification process.

Art Unit: 2763

As per claims 15-21, claim 15-21 are directed to a computer system for implementing the design verification process in claims 1-14, using a data structure to verify design files as taught by Ahmed; therefore, claims 15-21 are also rejected in like manner.

As per claims 16-25, due to the similarities of claims 16-25, and in addition the limitations of claims 1-14, Ahmed also discloses design rules files in templates for forming a set of global variables and setting/updating values for such variables for the design verification as claimed, thus, claims 16-25 are also rejected in like manner.

Conclusion

- 3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 1. Mahmood et al., "Datapath Synthesis Method and Apparatus Utilizing a Structured Cell Library", patent no. 5,519,627.
- 2. Warfield, Robert, "Automatic Software Testing Tool", patent no. 5,754,760.
- 3. Ooe et al., "Distribution File System for Accessing Required Portion of File", patent no. 5,761,498.
- 4. Shrote, Curtis, "Method and Apparatus for Generating Instruction/Data Streams Employed to Verify Hardware Implementations of Integrated Circuit Designs", patent no. 5,774,358.
- 5. Martineau et al., "Method and Apparatus for Establishing the Legitimacy of Use of a Block of Digitally Represented Information", patent no. 5,893,910.
- 6. Jain et al., "Visual Image Database Search Engine Which Allows for Different Schema", patent no. 5,911,139.
- 7. Steinman et al., "System and Method for Providing Encapsulated and Performance Efficient Data References in an Object Oriented Controller", patent no. 5,890,155.

Art Unit: 2763

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-1396 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

November 4, 1999

WESTERNIE STANDER
PARTIFE STANDER